Hardware Design Guide

AN7583GT / AN7583CT / AN7583DT/ AN7583ET
AN7553GT/ AN7553CT / AN7567GT / AN7567CT

Version: 1.2
Release date: 2024-09-18

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Design guide is subject to change without notice

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Contents

1 General information

1.1 Issue Control

This document was edited with Microsoft Word, Version 2007.

1.2 Record of Changes

Revision	etaDDateetaD	Author	Description
1.0	2024-03-06	KueiKC Wu	Initial version
1.0a	2024-04-16	Bin Tsou	Page9. Boot up strapping GPIO20 change to GbE Series Resistor. Page13. Add Combo-PON design. Page25. Update the Flash size support.
1.1	2024-05-27	Bin Tsou	Page12. XPON/XFI not used, the related power Do Not tie GND. Page14. PCIE0 not used, the related power Do Not tie GND.
1.2	2024-09-05	Bin Tsou	Page15. Separate the PCIE0/PCIE1 layout rule. Page15. SerDes4 add Ferrite bead for power noise isolation. Page17. SerDes5 add Ferrite bead for power noise isolation. Page25. DDR layout please follow the RFB & PCB stack up. Page26. Add Note2: EMMC_CMD & EMMC_D0 pull up requirement. Page27. EN7572/EN7573 LD+/- impedance requirement follow the AN. Page32. Add Maximum power consumption information. Page35. Add PCB_4Layer stack up for reference.

2 Introduction

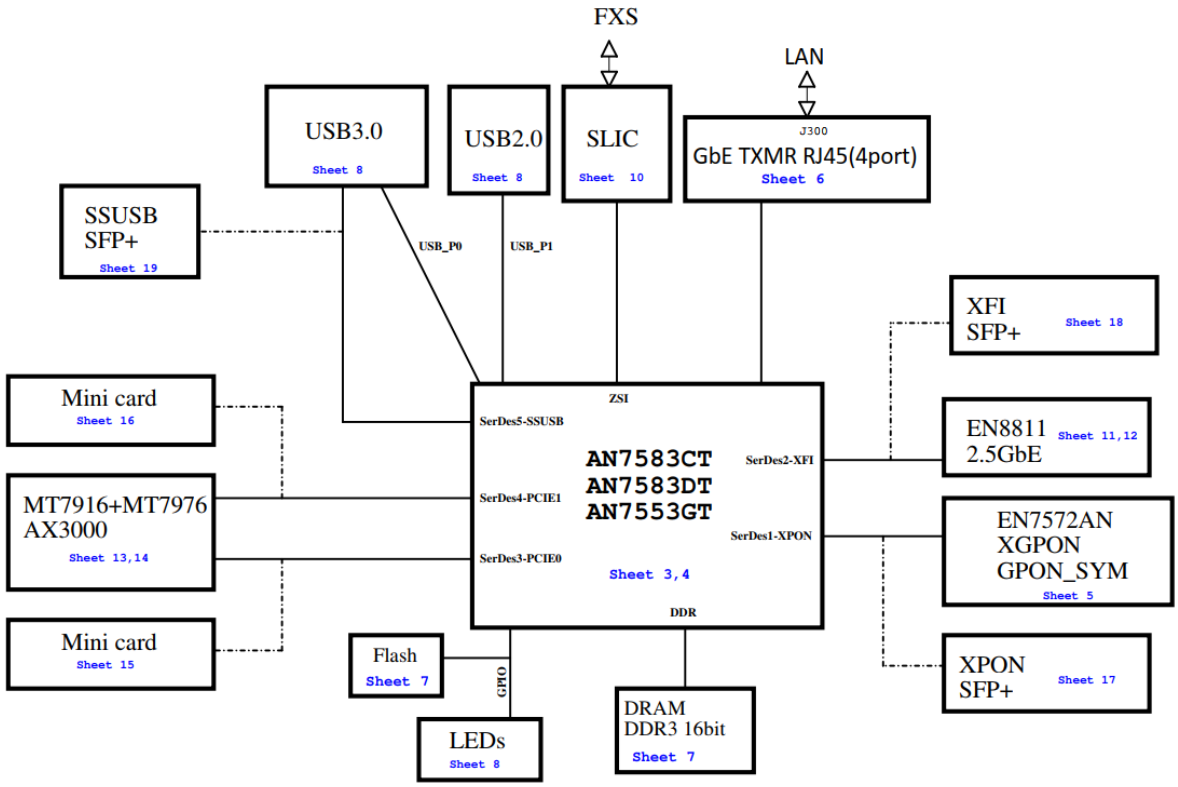
AN7583GT is a highly integrated single-chip solution for 10GEPON/XG-PON/XGS-PON/NG-PON2/EPON/GPON/Active Ethernet application. It integrates four Giga-bit Ethernet PHYs, one USXGMII interface, a DDR controller, one USB3.0 host interfaces, one USB2.0 host interface, one PCIe Gen3 RC, one PCIe Gen2 RC, and one PCM controller with ISI/ZSI compatible interface for VoIP application, supports SPI NOR/SPI NAND/Parallel NAND and eMMC, so that fully meets future smart home gateway requirements.

AN7583GT features a 1.2GHz ARM CA53 dual-core CPU and a powerful Xmart Packet Accelerator (XPA), which can support unmatched network features with extremely high packet processing capability. With XPA, AN7583GT performs an advanced QoS, security and flexible protocol management. By leading NP architecture and power-saving technology, AN7583GT makes system board design simple and easy, which can provide unique solution with low system cost and ultra-low power consumption in the market.

Please refer to Datasheet and “AN7583_AN7553_AN7567_Co-Design_Application_Note” for different model information.

3 Block diagram

ARH0170_AN7583CT+DDR3+MT7916-D25S



4 Key components

Part number	Description	Manufacturer
AN7583GT / AN7583CT / AN7583DT/ AN7583ET AN7553GT/ AN7553CT / AN7567GT / AN7567CT	xPON Processor	Airoha
EN7572/EN7573	10GPON LDD/LA	Airoha
W25M02GVZEIG W25N02KVZEIR	2GB SPI_NAND flash	Winbond
Le9643	1FXS VoIP access devices	Microsemi
XTL581130-A314-011	50MHz Crystal	Siward
W634GU6RB09I	DDR3L-2133 x16 4Gb	Winbond

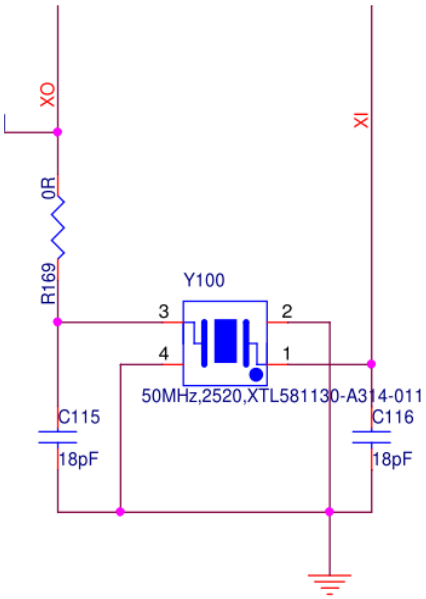
5 AN7583GT PON bridge/router processor

- Boot up Strapping of AN7583GT, default is internal pull-up. Use 4.7KΩ for pull low.

AN7583 Hardware Trap

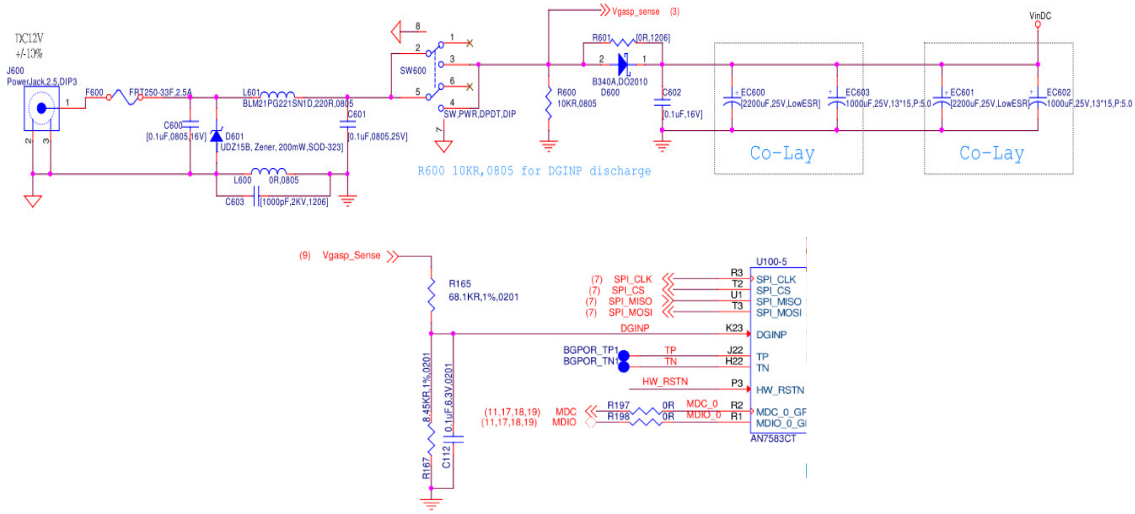
Pin Name	Description * means this board setting	IC Default
SPI_MOSI,SPI_CLK,SPI_MISO,UART_TXD	Boot_select: *1111: SPI NAND dummy append flash ECC 1100: SPI NAND dummy append controller ECC 1110: EMMC 0101: SPI NOR 3B mode 0100: SPI NOR 4B mode 1101: Parallel NAND Others : Reserved	4'b1111
GPIO0	boot_from_flash : 1'b0: disable (boot from internal ROM) *1'b1: enable (boot from flash)	1'b1
I2C0_SCL , SPI_CS	Option mode: 2'b00 : Do Not Use 2;b01 : Do Not Use 2;b10 : Do Not Use *2'b11 : Normal mode	2'b11
GPIO31,GPIO32	DDR select 2'b00: DDR3-1866 2'b01: DDR3-2133 *2'b10: DDR4-2666 2'b11: DDR4-3200	2'b11
GPIO20	GbE Series Resistor Select 1'b0: 0R *1'b1: 5R	1'b1

- AN7583GT CPU frequency is up to 1.2GHz dual-core.
- Please put crystal circuit close to AN7583GT & make sure it is within 50MHz +/-10ppm by tuning C115/C116 (Engineering sample RD tuning about 3 pcs PCB sample, 10ppm is not XTAL datasheet tolerance, it means actual measurement value)
- Support single-end clock input: XTAL_IN(ball J25) Tie to GND , and clock input to XTAL_OUT (J24) , the swing spec= 50MHz with 0.5V~1.8V Vp-p.

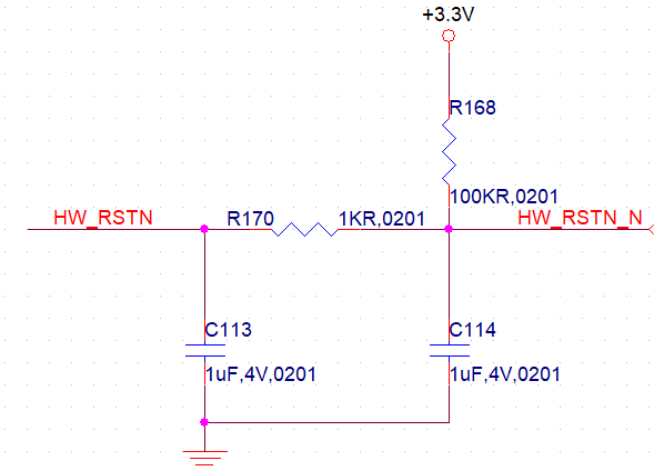


- Crystal Specification
  Please refer to Datasheet.

- AN7583GT incorporates comparator with on-chip reference for Dying Gasp function. The reference voltage is 1.0V +/-5%. If DGINP (Ball K23) is less than 1.0V +/-5%, it will trigger the Gasp function. (Note: C112 DGINP cap is for stability not for delay, please DO NOT remove it, and place it close to Ball K23)
  If Dying Gasp is not used, DGINP (Ball K23) please pull up to 3.3V by 4.7KR. (C112 CAP DO NOT remove.)
- Use 12Vdc power adaptor for Dying Gasp support



- SoC REXT_GBE (Ball F15) should through 24KR~24.3KR, 1% to GND and put it close to IC.
- AN7583GT incorporates Reset IC function. When 3.3V / Vcore is lower than a specific value, it will have a 20ms (typical value) low pulse to reset itself. It also can be reset by the Ball P3 (HW_RSTN) , HW_RSTN is 3.3V level , please pull up to 3.3V by 100KR resistor , connect 1uF CAP to GND and put it close to AN7583GT for stability.



- AN7583GT supports SPI_NOR / SPI_NAND / Parallel NAND / eMMC flash that can modify HW_Trap to select. AN7583GT RFB default uses SPI_NAND.

6 SerDes1 xPON / SerDes2 XFI interface

- AN7583GT SerDes1 xPON interface (Ball V24/V25/T24/T25) support XPON / XFI / USXGMII / HSGMII / SGMII
- AN7583GT SerDes2 XFI interface (Ball P24/P25/M24/M25) support XFI / USXGMII / HSGMII / SGMII

- xPON/XFI serdes is CML logic with AC coupled, both TX/RX need 0.1uF series CAP to device (If SFP+ module integrated CAP inside, there is no need to add on PCB side).
- xPON/XFI signals differential impedance are controlled at 90Ω.
- xPON/XFI signals P/N support the polarity reversal (P⇔N;N⇔P) by RG setting.
- If the xPON/XFI bus is not used, leave the bus not connect , the related power keep original power.
- xPON/XFI Serdes layout rule:

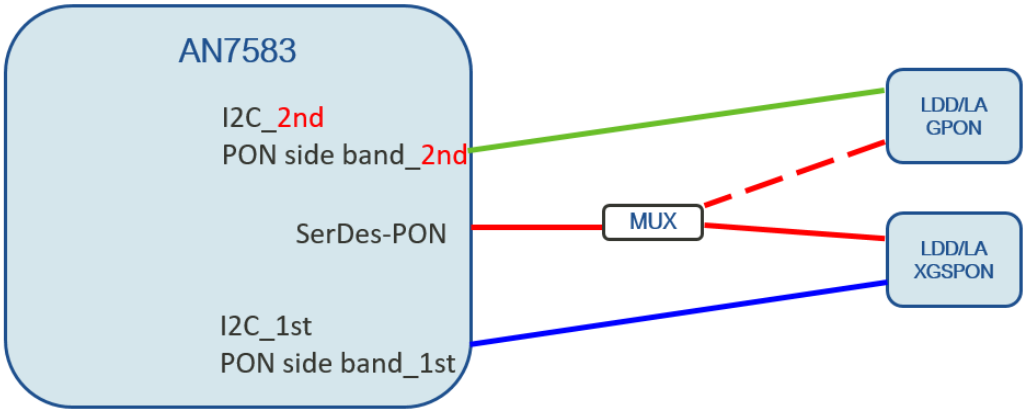
AN7583GT	Max. Speed	Impedance	Max. Length	aiVVia aiV allowed	Differential Pair trace /NPPWSKewks
xPON XFI USXGMII	10.3125Gbps	90R0R	hcinch	2	lim5millim5
HSGMII / SGMII	2.5G	90R0R	10 inch	2	lim5millim

Combo-PON design:

I2C & PON side band with independent I/O for combo-PON LDD/LA*2, save the cost of MUX (Legacy design MUX2).

PON side band_1st: Combo-PON XGSPON or Single PON application
PON side band_2nd: Combo-PON GPON application

AN7583 New Design



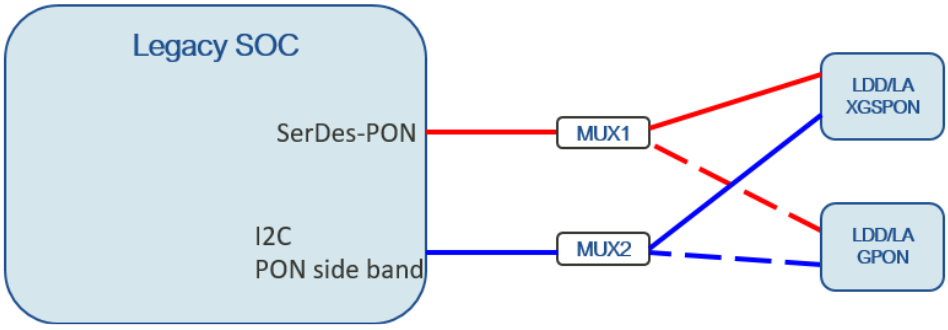
PON side band_1st:	Single PON or Combo-PON XGSPON
GPIO13	PON_RX_SD (I,HW)
GPIO14	PON_TX_SD (I,HW)
GPIO15	PON_TX_DIS (O,SW)
GPIO16	PON_RX_DIS (O,SW)
GPIO17	PON_TX_FAULT (B,HW)
GPIO18	PON_BURST_EN (O,HW)

I2C0_SCL / I2C0_SDA

PON side band_2nd:	Only for Combo-PON GPON
GPIO34	PON_TX_DIS (O,SW)
GPIO35	PON_RX_DIS (O,SW)
GPIO36	PON_RX_SD (I,HW)
GPIO37	PON_BURST_EN (O,HW)
GPIO38	PON_TX_SD (I,HW)

I2C1_SCL / I2C1_SDA

Legacy design



7 SerDes 3 PCIE0 / SerDes4 PCIE1 interface

- AN7583GT supports 1 port PCIe Gen3 host (PCIE0), 1 port PCIe Gen2 host (PCIE1)
- AN7583DT Do Not support PCIe function (xGMII supported).
- The SerDes3 PCIE0 also support USXGMII application.
- The SerDes4 PCIE1 also support HSGMII / SGMII application.
- There are only 3 modes for the 2 ports setting:

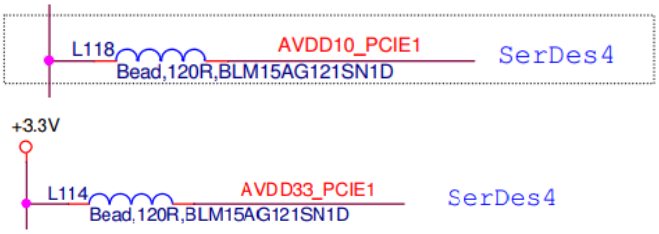
All w/o AN7583DT/ET	Mode 1	Mode 2	Mode 3	Not Support
SerDes3-PCIE0	PCIe G3/G2	PCIe G3/G2	USXGMII	USXGMII
SerDes4-PCIE1	PCIe G2	HSGMII(SGMII)	PCIe G2	HSGMII(SGMII)

AN7583ET	Mode 1	Mode 2	Not Support
SerDes3-PCIE0	NA	USXGMII	USXGMII
SerDes4-PCIE1	HSGMII(SGMII)	NA	HSGMII(SGMII)

Example: SerDes3 at USXGMII mode, SerDes4 used to be PCIe G2 or not used.
Do Not Support SerDes3: USXGMII + SerDes4: HSGMII simultaneously

- PCIE0/PCIE1 CLK P/N integrated 51R to GND inside the AN7583GT, PCB external 51R are reserved, default do not stuff.
- PCIE_RESET0 / PCIE_RESET1 default setting to open-drain (pull up at PCB side) for not 3.3V PCIE device application, it also can be config to push-pull 3.3V by software.
- PCIe signals should keep as short as possible. And make sure the PCB trace differential impedance are controlled at 85Ω for PCIE0 TX/RX , 90Ω for PCIE1 TX/RX , 100Ω for CLK.
- If the PCIE0 bus not used, leave the PCIe bus not connect, the related power keep original power.
- If the PCIE1 bus not used, leave the PCIe bus not connect, the related power can be connect to GND or keep original power.
- PCIE0/1 serdes is CML logic with AC coupled, PCIE0 TX/RX need 0.22uF series CAP to device, PCIE1 TX/RX need 0.1uF series CAP to device (If SFP+ module integrated CAP inside, there is no need to add on PCB side).
- Place the AC couple CAP 0.22uF(PCIE0) close to TX side for PCIE application, for others application place 0.1uF CAP.

- SerDes4: PCIE1 power add Ferrite bead for noise isolation & better performance.



- PCIE0/1 differential signal P/N support the polarity reversal (P⇔N;N⇔P) , PCIE function is auto detect , others controlled by RG setting
- PCIE0 Serdes Layout rule:

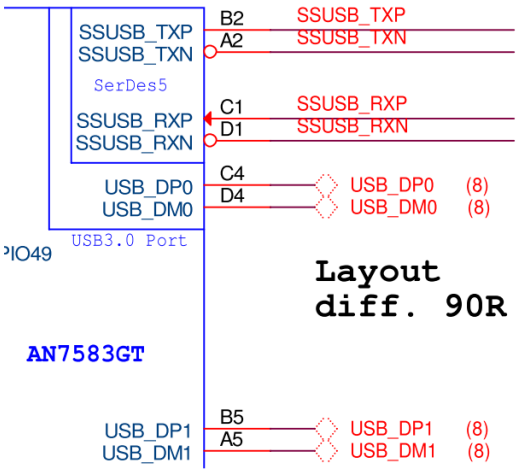
AN7583GT	Max. Speed	Impedance	Max. Length	Via allowed	Differential Pair trace P/N skew
USXGMII	0G110G0G1	90R/85R	5 inch	2	lim55millim5
PCIe Gen3/2	8.0Gbps	TX/RX: 5R885R5R8	8 inch (GEN3) 10 inch (GEN2)	2	lim55millim5
		CLK: R001100RR001	10 inch		(CLK < 60mil)

- PCIE1 Serdes Layout rule:

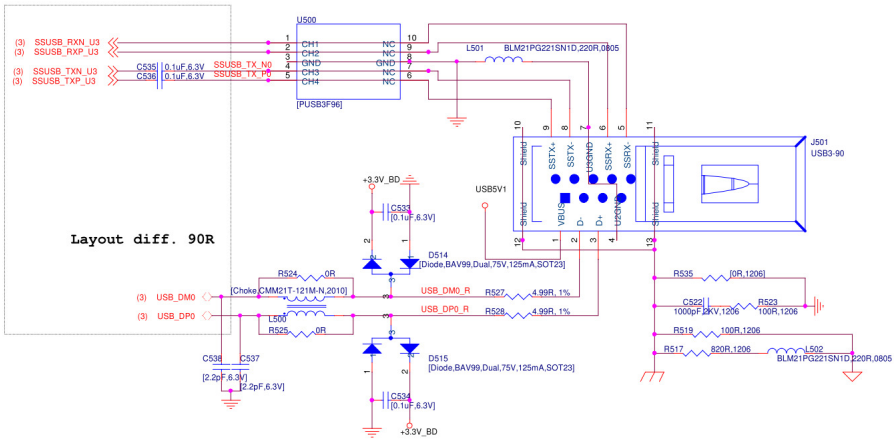
AN7583GT	Max. Speed	Impedance	Max. Length	Via allowed	Differential Pair trace P/N skew
PCIe Gen2	5.0Gbps	TX/RX: 0R990R0R9	10 inch	2	lim55millim5
		CLK: R001100RR001	10inchhcni		(CLK < 60mil)
HSGMII SGMII	5G.22.5G5G.2	0R990R0R9	10inchhcni	2	lim55millim5

8 SerDes5 SSUSB / USB Interface

- AN7583GT supports 1* USB3.0+2.0 Host port + 1* USB2.0 port.
- For USB3.0 application, the SSUSB+USB_DP0/DM0 is port0.
  Do Not use SSUSB+USB_DP1/DM1 for USB3.0.

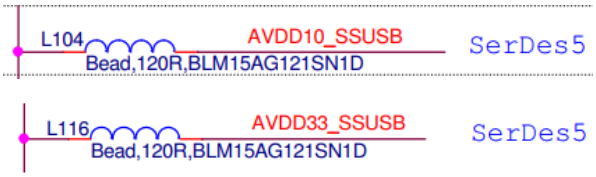


- SSUSB Serdes also support SGMII/HSGMII application.
- SSUSB serdes is CML logic with AC coupled, both TX/RX need 0.1uF series CAP to device. (For USB connector place at Host TX side only, USB device has cap at its TX side)
- When SSUSB config to SGMII/HSGMII function, the USB2.0 function is also workable.
- SSUSB differential signal P/N support the polarity reversal (P⇔N;N⇔P) by RG setting.
- SSUSB/USB signals should be controlled at 90Ω (Please see below figure).



- The USB2.0 series resistor 4.99R is recommend, and please also reserve BAV99 from 3V3 and GND at USB2.0 signals for ESD protection.

- Please have > 10mil space between USB_GND & System GND in PCB Layout.
- If do not use USB function, please leave the USB signals pin not connect , the related power can be connect to GND or keep original power.
- SerDes5: SSUSB/HSGMII power add Ferrite bead for noise isolation & better performance.



- It might need to add the ESD protector on USB signal for enhance ESD immunity.
- SSUSB / USB2.0 layout rule:

AN7583GT	Max. Speed	Impedance	Max. Length	Via allowed	Differential Pair trace P/N skew
USB2.0	480Mbps	0R990R0R9	10 inch	2	60mil
USB3.0 SGMII/HSGMII	5.0Gbps 1.25Gbps	0R990R0R9	10 inch	2	lim55millim5

9 Power-on sequence

■ Power-on sequence

AN7583 power on sequence requirement:

The power contains all of the AN7583+DRAM power (VCCK/AVDD10/1.8V/3.3V/VDDR etc.)

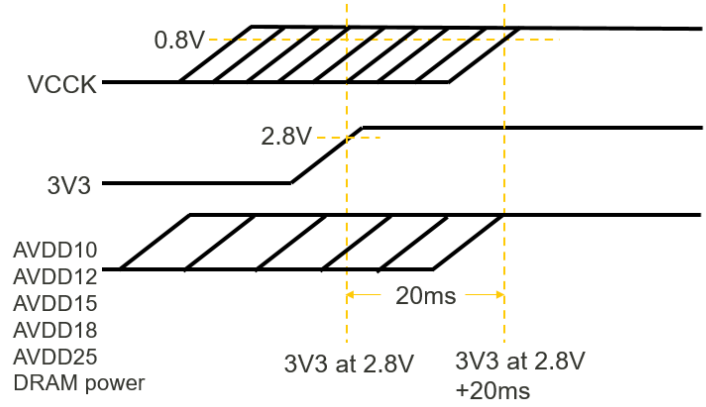
There is no sequence between VCCK and 3V3, others power need follow the sequence requirement below:

(1) **All of the AN7583+DRAM power ready before 3V3 rising to 2.8V +20ms**

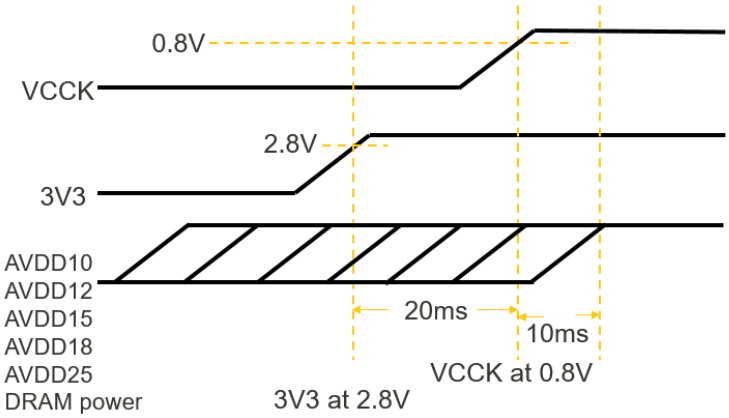
(2) **All of the AN7583+DRAM power ready before VCCK rising to 0.8V +10ms**

The condition (1) or (2) meet either one is OK.

Case 1: VCCK (at 0.8V) before 3V3 (at 2.8V) or after 3V3 (at 2.8V) within 20ms



Case 2: VCCK (at 0.8V) ready after 3V3 (at 2.8V) over 20ms

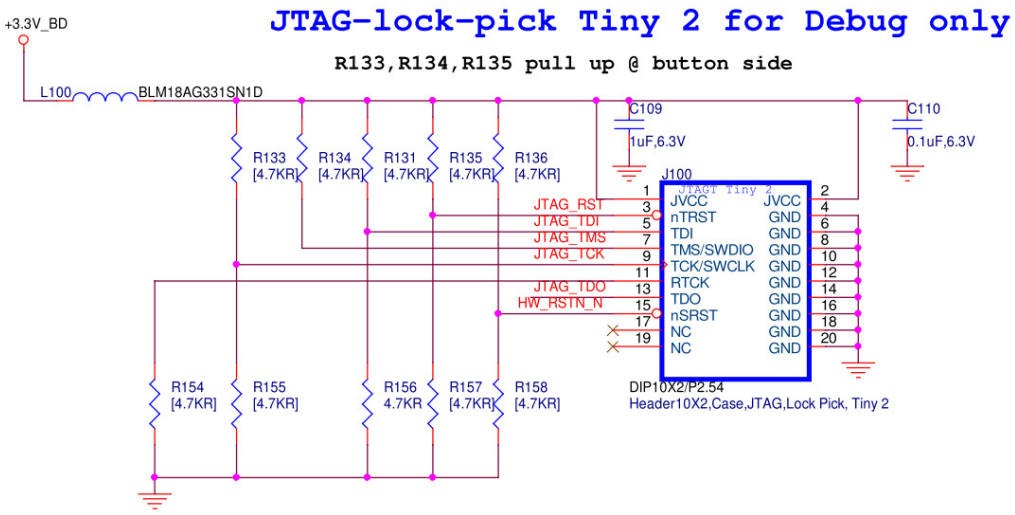


10 GPIO Usage / JTAG

- Please refer to the "ARH0170_AN7583CT_GPIO_table_V10_20240306.pdf" document for GPIOs usage.
- JTAG is enable default w/o external setting, please disable JTAG function for normal application (by FW).

- ARM EJTAG interfaces are including:
  - JTAG_RST
  - JTAG_DI
  - JTAG_DO
  - JTAG_MS
  - JTAG_CK

  Please follow below design for JTAG, if there is no enough space to place the connector, it should reserve the test point for debug purpose.



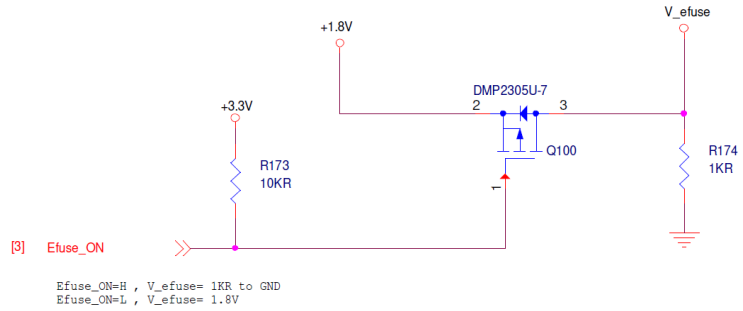
11 Efuse / AVS Design Guide

- AN7583GT EFUSE pin (Ball F22) design requirement:

◆ If there is no security key requirement to program , please tie it to GND directly.

◆ If security key is needed :

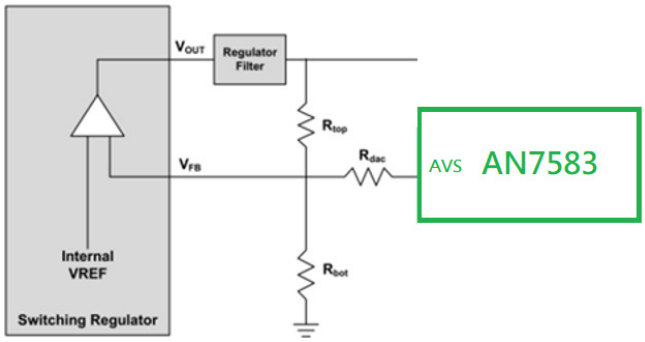
1. Connect the EFUSE pin to GND through 1KR resistor



2. When EFUSE write , connect EFUSE pin to power 1.8V +/-10% , when write finish , please remove the power.
   - ➢ It is recommend to use external Power supply 1.8V to Efuse pin when efuse write at production line , when write finish , remove the power.
   - ➢ If production line cannot use external power supply , use on board 1.8V +/-10% power through PMOS to switch on/off the efuse pin from power by GPIO19.
   - ➢ **Note : Please Do Not connect Efuse pin to power w/o Efuse write (Tie to GND directly or <1KR resistor to GND)**

➢ Efuse pin programing current about 50mA~100mA.

- AN7583GT AVS Design Guide:
  - ✧ **AVS Block diagram**



  - ✧ **AVS Schematic**

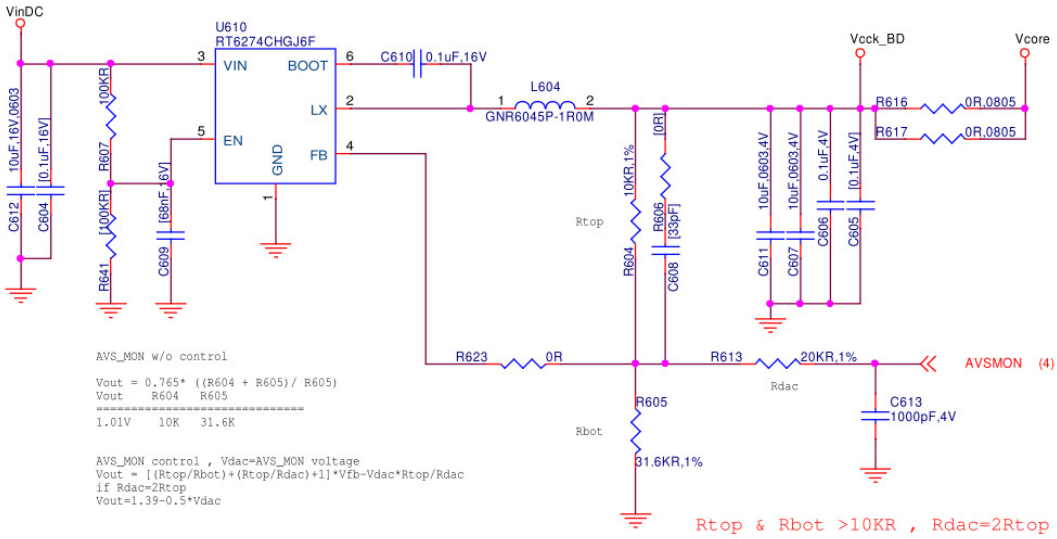
Spec: Rdac=2*Rtop , Rtop & Rbot >=10KR

The Buck regulator FB voltage range is 0.6V~0.8V

C613 for AVS_MON stability CAP value should be less than 1000pF

C613 Must place after R613, and should not place at FB pin.

SOC Core Power=1V with AVS



✧ Output Voltage Calculation

11.1.1 When AVS is not active, the AVSMON pin is Hi-Z

Vout = [(Rtop/Rbot)+1]*Vfb

11.1.2 When AVS active, the AVSMON will output voltage

Vout = [(Rtop/Rbot)+(Rtop/Rdac)+1]*Vfb – Vdac*Rtop/Rdac

Rdac=2*Rtop

Vout = [(Rtop/Rbot)+0.5+1]*Vfb – Vdac*0.5

Base on Rtop=10K , Rbot=31.6K , Vfb=0.765

Vout= 1.39-0.5*Vdac

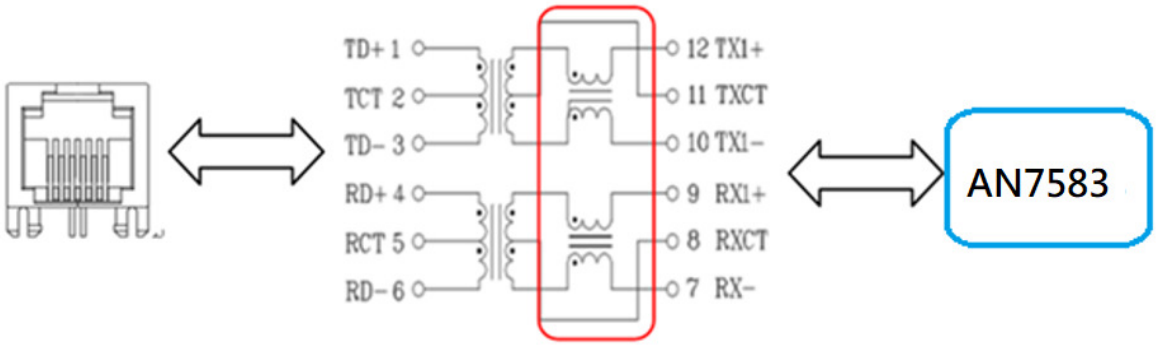
Note: Vdac is the voltage out of AVS pin (range from 0.1~1.3V)

Vout= 0.74~1.34V (Vfb=0.765V, so the limit cannot lower than 0.765V)

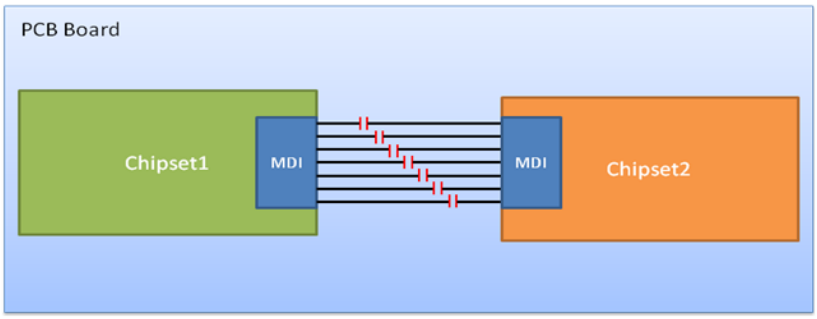
12 Ethernet Interface

- AN7583GT integrates 4 port Gigabit Ethernet PHYs .
- The MDI Bus should be controlled at differential 100Ω
- The differential pair P/N skew should be <50mil, pair to pair skew <1000mil
- Default use 4.99 ohm, 1% resistors on MDI Bus (between AN7583GT & Ethernet transformer) for Ethernet performance & surge protection.

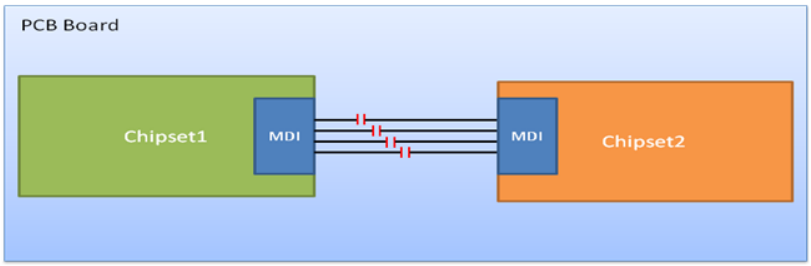
- For EMI test, please select Ethernet TXMR common choke close to AN7583 chip side.



- Suggest use 1uF capacitor for two chipset MDI connection on one PCB board.

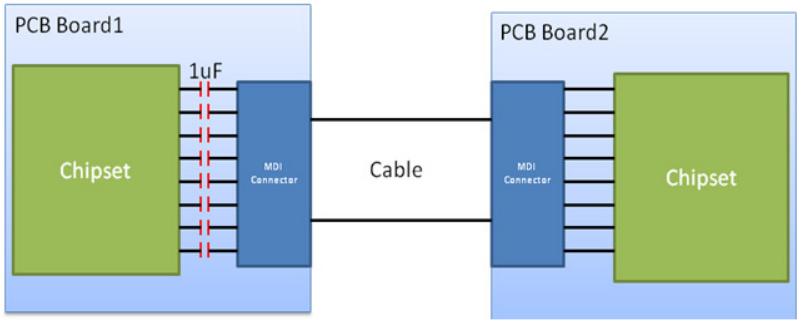


Gigabit Ethernet MDI Interface connection on one PCB board for two chipset



Fast Ethernet MDI Interface connection on one PCB board for two chipset

- Suggest use 1uF capacitor for two chipset MDI connection on two neighboring PCB board. Only one PCB reserve 1uF is enough



MDI Interface connection on two PCB board

13 Memory

13.1 SDRAM

- AN7583GT supports 16bit width DDR4 DRAM with BG1 can up to 4GB. Data rate up to 3200 Mbps.
- AN7583GT supports 16bit width DDR3 DRAM up to 512MB. Data rate up to 2133 Mbps
- DDR layout rule:
  - Please 100% copy the reference design's layout directly.
  - The PCB stack up please follow the RFB.
  - RFB is 2 Layer layout. > 2 Layer layout can be modified by adding GND & Power planes separately.

- For DDR support list please reference DDR support list file "AIROHA_AN7583GT_DDR_Support_List_Vxx.pdf".

13.2 Flash

- AN7583 supports SPI_NOR flash up to 256Mbit
- AN7583 supports SPI NAND / Parallel NAND page size 2KB or 4KB, SPI NAND up to 8Gbit , Parallel NAND up to 16Gbit
- AN7583 supports eMMC spec v4.4 , up to 16GByte.
- AN7583 SPI_NAND support both flash ECC and SOC ECC.
- The following table is the boot strap for SPI_NOR & SPI_NAND & eMMC & Parallel NAND flash.

AN7583 Hardware Trap

Pin Name	Description * means this board setting	IC Default
SPI_MOSI,SPI_CLK,SPI_MISO,UART_TXD	Boot_select: *1111: SPI NAND dummy append flash ECC 1100: SPI NAND dummy append controller ECC 1110: EMMC 0101: SPI NOR 3B mode 0100: SPI NOR 4B mode 1101: Parallel NAND Others : Reserved	4'b1111

- For flash support list please reference" TBD" .

13.3 SPI / EMMC / Parallel NAND pin assignment

Pin Name	SPI	eMMC	Parallel NAND	Parallel NAND TSOP48
SPI_CS	1st SPI_CS0	eMMC_RESET	NFD_ALE	Pin17
SPI_CLK	1st SPI_CLK	eMMC_CLK	NFD_CLE	Pin16
SPI_MOSI	1st SPI_MOSI	eMMC_CMD(Note2)	NFD_WEN	Pin18
SPI_MISO	1st SPI_MISO		NFD_CSN_0	Pin9
GPIO5		eMMC_DAT0(Note2)	NFD_CSN_1(Note1)	Pin10
GPIO6		eMMC_DAT1	NFD_RBN_1(Note1)	Pin6 , pull up 10KR to 3V3
GPIO7		eMMC_DAT2	NFD_RBN	Pin7 , pull up 10KR to 3V3
GPIO20		eMMC_DAT3	NFD_DATA0	Pin29
GPIO21		eMMC_DAT4	NFD_DATA1	Pin30
GPIO22	2nd SPI_CS1	eMMC_DAT5	NFD_DATA2	Pin31
GPIO23	1st SPI_WP_N	eMMC_DAT6	NFD_DATA3	Pin32
GPIO24	1st SPI_HOLD_N	eMMC_DAT7	NFD_DATA4	Pin41
GPIO25	1st SPI_CS1		NFD_DATA5	Pin42
GPIO26	2nd SPI_CLK		NFD_DATA6	Pin43
GPIO27	2nd SPI_CS0		NFD_REN	Pin8
GPIO28	2nd SPI_MOSI		NFD_DATA7	Pin44
GPIO29	2nd SPI_MISO		NFD_WP	Pin19, pull up 10KR to 3V3

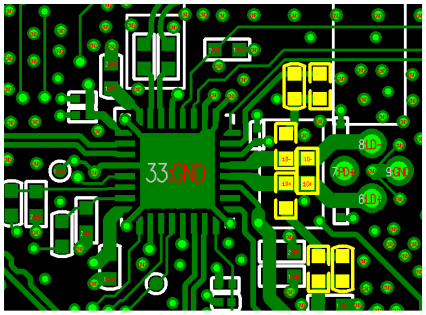
- Note1: When Parallel NAND w/o CSN_1 / RBN_1, GPIO5/6 can be used to GPIO function.
- Note2: Please add pull-up Resistor 10KR for EMMC_CMD , EMMC_D0.

14 EN7572 / EN7573 10G LDD/LA BOSA On BOARD

- EN7572 is designed for XGPON & XEPON Asymmetric 10G PON application.
- EN7573 is designed for XGSPON & XEPON Symmetric 10G PON application.
- EN7572 / EN7573 are pin to pin design.
- XPON Connection topology :
  AN7583GT XPON_TX ⇔ 0.1uF CAP ⇔ EN7572/EN7573 TXIN
  AN7583GT XPON_RX ⇔ 0.1uF CAP ⇔EN7572/EN7573 RXOUT
  Please follow the XPON interface 10G layout rule.
- TXOUTN (LD+) / TXOUTP(LD-) is Laser diode drive for BOSA LD , impedance control follow the newest "Design_Application_Note" , trace length is as short as possible , Length< 280mil, the matching component pad on the trace, w/o unnecessary trace.

For more detail information, please refer to "EN7572_EN7573_Design_Application_Note"

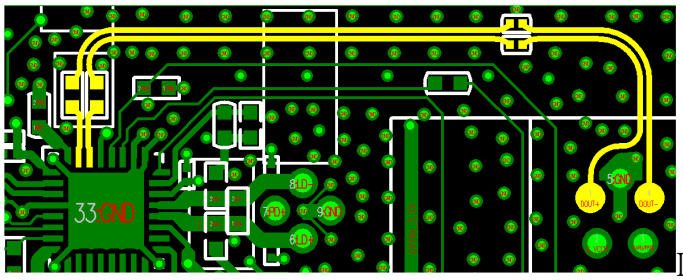
	Max. Speed	Impedance	Max. Length	Via allowed	Differential Pair trace P/N skew
LD+/-	2.488Gbps (XGPON) 1.25Gbps(XEPON_ASY)	Application note for detail	280mil	X	5mil
	10.3125Gbps (XEPON_SY) 9.95328Gbps (XGSPON)		175 mil		



LD+/- (pin20,21)

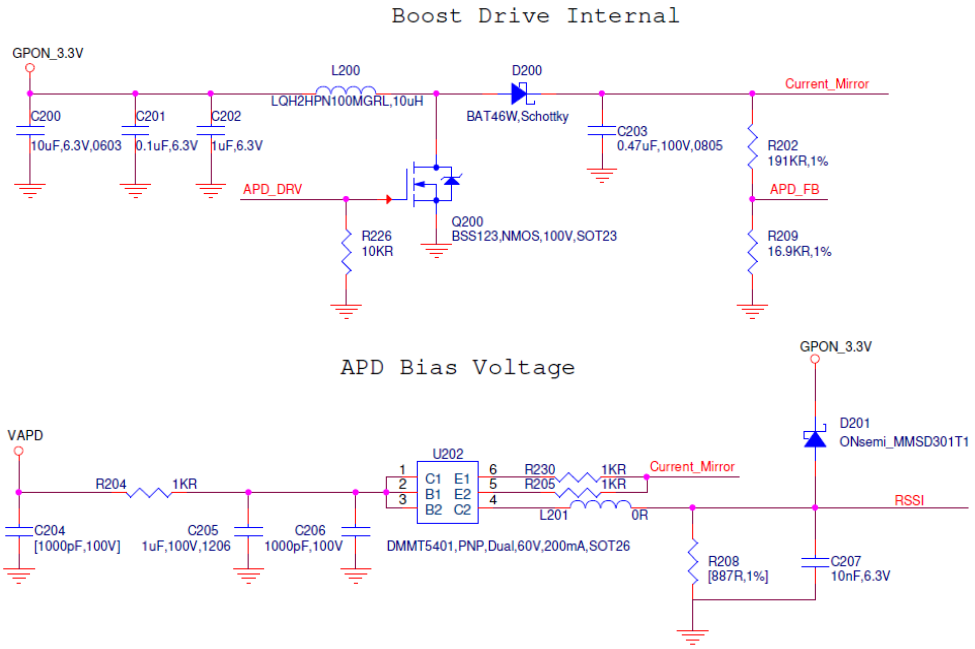
- RXINN (Dout-) / RXINP (Dout+) is RX input from BOSA, please add series 0.1uF CAP , and reserve the 0 ohm for RX-Desense from noise , impedance is 90 ohm differential trace length <1.7 inch.

	Max. Speed	Impedance	Max. Length	Via allowed	Differential Pair trace P/N skew
Dout+/-	10.3125Gbps	90R differential	1.7 inch	X	5mil



Dout+/-(pin 30,31)

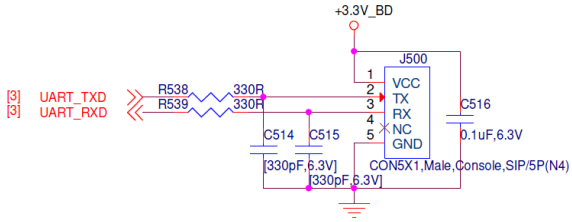
- Please keep “clearance “for these four pairs (XPON TX/RX , LD , Dout).
- BSS123(Q200) and R226 should be close to pin APD_DRV(U200.8)
- The inductor (L200), diode (D200) and 0.47uf, 100V output capacitor (C203) should be close to the Q200.
- U200.32 (IREF pin) must connect to 24.3kΩ, 1% resistor (R220) and R220 must close to U200.32.
- Reserved C247,C248 cap close to U200.22 & C231, C249, C250 cap close to BOSA
- For 10GPON BOSA application, the BOSA RX needs the APD bias voltage.
  Please follow the HDK design for APD_FB, RSSI is the Current Sense pin for APD , the CAP C207 place close to U200.28 RSSI pin , the diode D201 MMSD301T1 is protection device for RSSI .



15 UART / CONSOLE / LED

15.1 UART / Console

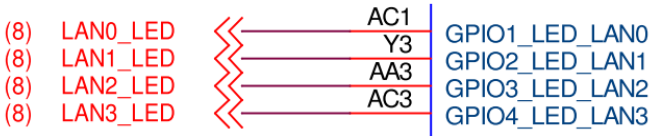
- AN7583 supports 5 UART ports (GPIO Shared).
- UART_TXD / UART_RXD (ball AE2/AF2) is for Console only.
- J500 is AIROHA console port connector. System vendor should change to their own console port connector. C514 & C515 is for EMI/ESD solution. It should not greater than 330pF. R538/R539 is for ESD protection, it should not greater than 330R.
- J500 should place away from serdes signals to avoid interference.



- Others UART ports shared with GPIO , please reference datasheet for more detail.

15.2 LED

- Default use low active for LED function.
- GPIO31/32/20 are HW trap pin , please use low active LED when HW trap pull up , use high active when pull down.
- Please note, some GPIO has HW function for LED. If need use EPHY HW light on LED, should connect to corresponding GPIO. (Port 0 using LAN0_LED , …. , Port3 using LAN3_LED)



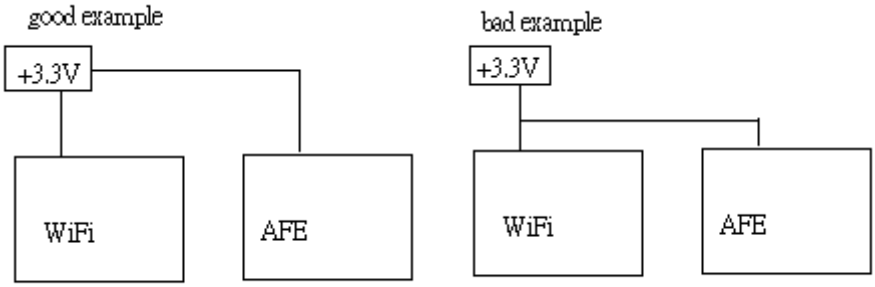
- The LED function supports TR-068 & CTC E8C LED. The 100pF capacitor is reserved for ESD/EMI.
- GPIO20~24 default for JTAG, can be disable by FW, if the LED cannot accept blink instantly at power on step, please prevent to use these GPIO pin for LED.
- GPIO49~50 default for PCIE reset, suggest to use high active LED.

16 IAD

- AN7583 can support SLIC with up to 2FXS & 1 FXO(or 4FXS). It has 1* ISI/ZSI interface (share with PCM interface).
- Microsemi Le9642/Le9641/Le9643 & Silicon Labs Si32266/Si32193 are supported.
- For SLIC system design, please follow SLIC's design guideline.
- Put decoupling capacitors near IC power/ground pins
- SLIC will generate noise that will affect PON signal. SLIC circuit should put away from PON interfaces.

17 Wi-Fi

- Put decoupling capacitors near IC power/ground pins
- For WiFi system design, please follow MeadaiTek WiFi reference design guideline.
- The WiFi Layout is recommended 100% copy from Reference Design.
- The WiFi power trace should use star topology. (Especially for 2layer PCB)



18 Power

18.1 Chip power consumption

■ Maximum power consumption of AN7583GT

AN7583GT DDR4	Vcore 1.0V	AVDDK 1.0V	DRAM 1.2V	DRAM 2.5V	1.8V	3.3V
Current(mA)	1800	350	180	45	120	240

AN7583GT DDR3	Vcore 1.0V	AVDDK 1.0V	DRAM 1.5V	1.8V	3.3V
Current(mA)	1800	350	180	160	240

Note:

The maximum current consumption (with Typ. voltage) is defined under the condition: IC junction temperature < 125˚C, all interfaces are in busy state. The maximum power consumption is 3.5W in this condition.

18.2 Typical power consumption of evaluation board (CoC)

TBD

19 Layout

19.1 Placement

- Place decoupling capacitor close to IC's power pin.
- Keep signal flow as direct as possible.
- Keep switching power away from high speed or critical signals.
- Place crystal close to IC's XIN/XOUT pin.
- Keep optical transceiver pins 20mil space away the GND plane.
- Keep PON TX & RX differential signals 90 ohm impedance match.
- AN7583GT need Heat sink. Consider the heat sink space when PCB Placement. In our RFB use 59x59x12mm
- Both AN7583GT & WIFI Chips & Other Chips are hot spot, place them away from each other was strongly recommended.

19.2 Critical signal

- Differential signals
  - xPON / XFI / PCIE / SSUSB serdes and USB2.0 signals
  - DOUT+/- from PON BOSA
  - TXVP/TXVN EPHY MDI

- Sensitive Signals
  - LD+/- for LDD/LA TX signals.
  - PON_BURST_EN
  - DRAM signals
  - XIN/XOUT XTAL signals

19.3 Ground/Power plane Separation

- Reference ground/power plane separation, please refer to gerber file.

19.4 Layer stack up and routing

- Reference layer stack up (total thickness 1.6mm)

PCB: 2 Layer

Layer	Type		Thickness (mil)			DK
Top side solder mask				0.80	mils	
L1	TOP	Differential & Signal	copper+plating	1.40	mils	
			core	57.75	mils	4
L2	Bottom	Differential & Signal	copper+plating	1.40	mils	
Bottom side solder mask				0.80	mils	
TOTAL				62.15	mils	
				1.58	mm	

Impedance

Single end					Diff				
線寬 / 線距(mil)	線寬 / 線距(mm)	參考層	ohm值(±10%)	理論值	線寬 / 線距(mil)	線寬 / 線距(mm)	參考層	ohm值(±10%)	理論值
22(gap5mil)	0.5588/(gap0.127)	L2	50	50.18	8/4.5(gap5mil)	0.2032/0.1143 (gap0.127)	L2	90	89.88
50(gap5mil)	1.27(gap0.127)	L2	40	40.2	5/4.5(gap5mil)	0.127/0.1143 (gap0.127)	L2	100	100.47
10.5(gap5mil)	0.2667(gap0.127)	L2	60	59.96	9.5/4.5(gap4.5mil)	0.2413/0.1143 (gap0.1143)	L2	85	
					8/4.5(gap5mil)	0.2032/0.1143 (gap0.127)	L1	90	89.88
					5/4.5(gap5mil)	0.127/0.1143 (gap0.127)	L1	100	100.47
					9.5/4.5(gap4.5mil)	0.2413/0.1143 (gap0.1143)	L1	85	

PCB: 4 Layer

PCB Stack Up							Impedance										
Layer	Type		Thickness (mil)			DK	Single end					Diff					
Top side solder mask				0.80	mils		線寬 / 線距(mil)	線寬 / 線距(mm)	參考層	ohm值(±10%)	理論值	線寬 / 線距(mil)	線寬 / 線距(mm)	參考層	ohm值(±10%)	理論值
L1	TOP	Differential & Signal	copper+plating	1.40	mils		7.5(gap7.5mil)	0.1905/(gap0.1905)	L2	50	49.71	6/4.5(gap5mil)	0.1524/0.1143(gap0.127)	L2	85	85.7
							24(gap7.5mil)	0.6096(gap0.1905)	L2	25		5/4.5(gap4.5mil)	0.127/0.1143(gap0.1143)	L2	90	90.59
												4.5/5.5(gap5mil)	0.1143/0.1397(gap0.127)	L2	100	99.57
			Prepreg	4.85	mils	3.98										
L2		GND	copper	1.25	mils							4/6.5(gap8mil)	0.1016/0.1651(gap0.2032)	L1/L3	100	100
			core	44.50	mils	4										
L3		VCC	copper	1.25	mils		6(gap7mil)	0.1524/(gap0.1778)	L1/L3	50	49.55	6/6.5(gap7mil)	0.1524/0.1651(gap0.1778)	L2/L4	85	85.45
												5/6(gap8mil)	0.127/0.1524(gap0.2032)	L2/L4	90	90.7
												4/6.5(gap8mil)	0.1016/0.1651(gap0.2032)	L2/L4	100	100
			Prepreg	4.85	mils	3.98										
L4	Bottom	Differential & Signal	copper+plating	1.40	mils		7.5(gap7.5mil)	0.1905/(gap0.1905)	L3	50	49.71	6/4.5(gap5mil)	0.1524/0.1143(gap0.127)	L3	85	85.7
												5/4.5(gap4.5mil)	0.127/0.1143(gap0.1143)	L3	90	90.59
Bottom side solder mask				0.80	mils											
TOTAL				61.10	mils											
				1.55	mm											

- Default trace width / spacing: 4 mil / 4 mil
- Default power / ground trace width: >=25 mil if possible
- Use GND as guard trace for high speed digital signal.
- Routing high speed digital signal without VIA is preferred
- Keep differential signals as close (5mil spacing, if no impedance controls need) & symmetry as possible.
- Keep analog & differential signals away from high speed digital signals.
- Use 12mil width with Guard trace for clock signals.